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BRADLEY K DESANDRO
WORKMAN NYDEGGER & SEELEY
1000 EAGLE GATE TOWER
60 EAST SOUTH TEMPLE
SALT LAKE CITY, UT 84111

EXAMINER	
GOUDREAU, GEORGE A	
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Please find below and/or attached an Office communication concerning this application or proceeding.

53

Office Action Summary

Application No.	Applicant(s)
09-559,504	Donohoe et al.
Examiner	**Group Art Unit**
George Goudreau	1763

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

☒ Responsive to communication(s) filed on 5-02-01 (Ce, - paper # 4)

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 1-49 is/are pending in the application.

Of the above claim(s) 7, 20, 48 is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-6, 8-19, 21-47, 49 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claim(s) _____ are subject to restriction or election requirement

Application Papers

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119 (a)-(d).

☐ All ☐ Some* ☐ None of the:

☐ Certified copies of the priority documents have been received.

☐ Certified copies of the priority documents have been received in Application No. _____.

☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a))

*Certified copies not received: _____.

Attachment(s)

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 2

☒ Notice of Reference(s) Cited, PTO-892

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Interview Summary, PTO-413

☐ Notice of Informal Patent Application, PTO-152

☐ Other _____

Office Action Summary

15. Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5 should depend upon claim 3 instead of claim 4 in order to have proper antecedent basis.

16. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

17. Claims 1-2, 6, 8-9, and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Yang et. al. (6,194,325).

Yang et. al. disclose a process for selectively rie etching a generic oxide layer (i.e.- SiO2) to an underlying generic nitride layer (i.e.-Si3N4) on a wafer in a plasma comprised of a hydrocarbon gas (i.e.- CHF3, CH2F2, or CH3F), and a fluorocarbon (i.e.- CF4, C2F6, or C3F8). The plasma is formed in the rie etcher using an RF inductively coupled coil (300) which surrounds the plasma generation chamber (17 W). The etcher is equipped with third electrode (i.e.-a RF biased, solid Si electrode (17 S)) which is used to scavenge free F in fluorocarbon based plasma in

order to increase the selectivity of the SiO2 etch relative to the Si3N4 etch stop layer. This is discussed specifically in general in columns 4-8; and discussed in columns 1-12. This is shown in figures 1-2.

18. Claims 1-3, 5, and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Rhoades et. al. (5,269,879).

Rhoades et. al. disclose a process for selectively rie etching a SiO2/Si3N4 ILD (11) to an underlying TiN metal wiring layer (2) on a wafer using a patterned photo resist etch mask (12), and a plasma comprised of at least one of CF4, CHF3, C2F6, CH2F2, and/or SF6 plus a N2 passivant gas. A carrier gas such as Ar, He, Ne, Kr, may optionally be present in the plasma etchant. This is discussed specifically in columns 3-6; and discussed in general in columns 1-8. This is shown in figures 1-3.

19. Claims 1-2, 6, 9, 14-16, 19, 42-43, and 46 are rejected under 35 U.S.C. 102(e) as being anticipated by Yang et. al. (6,227,211).

Yang et. al. disclose a three step etching process for form a SAC by selectively etching a SiO2 ILD layer to an underlying Si3N4 layer using a patterned photo resist etch mask, and the following sequence of etch steps:

-First the SiO2 ILD layer is rie etched in a bulk etching step which employs a plasma comprised of (CH2F2-C4F8-CO).;

-Second, the SiO2 ILD is selectively etched to an underlying Si3N4 layer using a plasma comprised of (CH2F2-C4F8-C2F6-CO-O2-Ar).; and

-Third the SiO2 ILD is over etched in a plasma comprised of (CH2F2-C4F8-CO).

This is discussed specifically in columns 4-5; and discussed in general in columns 1-8. This is shown in figures 1-5.

20. Claims 1-2, 6, and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Lin et. al. (5,880,006).

Lin et. al. disclose a process for selectively rie etching a SiO2 layer to a Si3N4 etch stop layer using a plasma comprised of (CHF3-CF4) to form SiO2 sidewall spacers (72) on the sidewalls of gates (64) on the surface of a wafer. This is discussed specifically in columns 4-5; and discussed in general in columns 1-6. This is shown in figures 1-10.

21. Claims 1-2, 6, 9, and 14-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Nulty (5,562,801).

Nulty discloses a two step etching process for forming a SAC (1522) in an ILD layer (1501) on the surface of a wafer (1500). The ILD layer is comprised of TEOS SiO2/BPSG. The first etching step employs a photo resist (1510)/ hard mask (1505) etch mask. The second etching step employs a hard mask (1505) etch mask. The first etching step employs a plasma comprised of (CHF3-C2F6). The second etching step employs a plasma comprised of (CHF3-C2H2F4). The photo resist etch mask (505) is stripped off of the wafer surface between the first, and second

etching steps. The second etching steps is conducted until it contacts a Si3N4 layer (1503) on the sides of a gate (1503) which behaves as a type of sidewall spacer. This is discussed specifically in columns 7-13; and discussed in general in columns 1-16. This is shown specifically in figures 15-17; and shown in general in figures 1-20.

22. Claims 1-2, 6, 9, 14-16, 19, 26, and 29 are rejected under 35 U.S.C. 102(e) as being anticipated by Marquez et. al. (6,133,153).

Marquez et. al. disclose a two step rie etching process for forming a SAC (44) in an ILD layer (40) on the surface of wafer (22). The SAC is formed between two gates (28, 33) which are on the surface of the wafer . Both etching steps employ a patterned photo resist layer (42). The first etching step etches a first portion of the SiO2 ILD, and employs a plasma comprised of (C2F6-C2HF5) with CH2F2 optionally being present. The second etching step employs a plasma comprised of (C4F8-CH2F2) with either of (C2F6 or CF4) optionally being present. The second etching steps is conducted until it contacts the Si3N4 etch stop layer (32, 34). The Si3N4 layers (32, 34) function as a type of sidewall spacer on the surface of the gates (24, 26) on the surface of the wafer. This is discussed specifically in columns 9-10; and discussed in general in columns 1-12. This is shown in figures 1-5.

23. Claims 1-3, and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Kuo et. al. (6,063,709).

Kuo et. al. disclose a process for rie etching a SOG (16) / SiO2 (12) ILD layer until the surface of a TiN AR, etch stop layer (15) on a wafer (11) is reached using a plasma which is comprised of (CF4-CHF3-Ar). The TiN AR etch stop layer covers a wiring layer (14) on the surface of a wafer. This is discussed specifically in columns 2-3; and is discussed in general in columns 1-4. This is shown in figures 1-3.

24. Claims 1-2, 6, 9 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Blalock et. al. (5,286,344).

Blalock et. al. disclose a process for selectively rie etching a SAC in a SiO2 ILD (14) to an underlying Si3N4 layer (16) on the surface of wafer using a patterned photo resist layer (12), and a plasma comprised of any of CHF3, CF4, or Ar plus any of CH2F2, CH3F. The Si3N4 layer covers two polysi gates (17) on the surface of the wafer. The polysi gates are surrounded by SiO2 sidewall spacers (19). This is discussed specifically in columns 6-8; and discussed in general in columns 1-12. This is shown in figures 1-2.

25. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

26. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103© and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

27. Claims 3-5, 10-12, 36-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et. al. as applied in paragraph 17 above.

Yang et. al. as applied in paragraph 17 above fail to disclose the following aspects of applicant's claimed invention:

-the specific usage of TiN as the etch stop layer in place of the Si3N4 etch stop layer specifically taught above;

-the specific usage of a Si ring on the cathode in the rie etcher which surrounds the wafer during the rie etching process, and is used to scavenge free F in the plasma etchant; and

-the specific usage of applicant's claimed etching process parameters

It would have been obvious to one skilled in the art to replace the Si3N4 etch stop layer in the process taught above with a TiN etch stop layer based upon the following. The usage of TiN etch stop layers when etching vias in SiO2 ILD layers is conventional or at least well known in the semiconducting arts. (The examiner takes official notice in this regard.) Further, this simply provides an alternative, and at least equivalent means for providing a nitride etch stop means in etching process taught above to those means which are specifically taught above (i.e.- a Si3N4 etch stop.)

It would have been obvious to one skilled in the art to employ a Si ring on the cathode in the rie etcher taught above during the rie etching process based upon the following. The usage of a Si ring on a cathode which surrounds a wafer to be etched in a fluorocarbon based plasma during the selective etching of an oxide based layer to a nitride based layer is conventional or at least well known in the etching arts. (The examiner takes official notice in this regard.) Further, this would simply provide a means for further desirably increasing the etch selectivity of the oxide based layer to the nitride based layer in the etching process taught above.

It would have been prima facie obvious to employ any of a variety of different etch process parameters in the etching process taught above including those which are specifically claimed by the applicant. These are all well known variables in the plasma etching art which are known to effect both the rate and quality of the plasma etching process. Further, the selection of

particular values for these variables would not necessitate any undo experimentation which would be indicative of a showing of unexpected results.

Alternatively, it would have been obvious to one skilled in the art to employ the specific etch process parameters which are claimed by the applicant in the etching process taught above based upon In re Aller as cited below.

"Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F. 2d 454, 105 USPQ 233, 235 (CCPA).

Further, all of the specific etching process parameters which are claimed by the applicant are results effective variables whose values are known to effect both the rate, and the quality of the plasma etching process.

28. Claims 4, 8, 10-12, and 36-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rhoades et. al. as applied in paragraph 18 above.

Rhoades et. al. as applied in paragraph 18 above fail to disclose the following aspects of applicant's claimed invention:

-the specific usage of a solid Si electrode (i.e.-a Si roof in the plasma etching chamber) to scavenge free F in the plasma etchant during the plasma etching process;

-the specific usage of a Si ring on the cathode in the rie etcher which surrounds the wafer during the rie etching process, and is used to scavenge free F in the plasma etchant; and

-the specific usage of applicant's claimed etching process parameters

It would have been obvious to one skilled in the art to equip the rie etching apparatus employed in the plasma etching process taught above with a solid Si electrode which forms the roof of the plasma etching chamber based upon the following. The usage of such a solid Si electrode to scavenge free fluorine in a fluorocarbon based plasma used to selectively rie etch an oxide layer to a nitride layer is conventional or at least well known in the plasma etching arts. (The examiner takes official notice in this regard.) Further, this would simply provide a means for further desirably increasing the etch selectivity of the oxide based layer to the nitride based layer in the etching process taught above by scavenging free fluorine in the plasma etchant.

It would have been obvious to one skilled in the art to employ a Si ring on the cathode in the rie etcher taught above during the rie etching process based upon the following. The usage of a Si ring on a cathode which surrounds a wafer to be etched in a fluorocarbon based plasma during the selective etching of an oxide based layer to a nitride based layer is conventional or at least well known in the etching arts. (The examiner takes official notice in this regard.) Further, this would simply provide a means for further desirably increasing the etch selectivity of the oxide based layer to the nitride based layer in the etching process taught above.

It would have been prima facie obvious to employ any of a variety of different etch process parameters in the etching process taught above including those which are specifically claimed by the applicant. These are all well known variables in the plasma etching art which are

known to effect both the rate and quality of the plasma etching process. Further, the selection of particular values for these variables would not necessitate any undo experimentation which would be indicative of a showing of unexpected results.

Alternatively, it would have been obvious to one skilled in the art to employ the specific etch process parameters which are claimed by the applicant in the etching process taught above based upon In re Aller as cited below.

"Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F. 2d 454, 105 USPQ 233, 235 (CCPA).

Further, all of the specific etching process parameters which are claimed by the applicant are results effective variables whose values are known to effect both the rate, and the quality of the plasma etching process.

29. Claims 4, 8, 21, 23-30, 32-33, 35, 47, and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et. al. as applied in paragraph 19 above.

Yang et. al. as applied in paragraph 19 above fail to disclose the following aspects of applicant's claimed invention:

-the specific usage of TiN as the etch stop layer in place of the Si3N4 etch stop layer specifically taught above;

-the specific usage of a solid Si electrode (i.e.-a Si roof in the plasma etching chamber) to scavenge free F in the plasma etchant during the plasma etching process;

-the specific usage of a Si ring on the cathode in the rie etcher which surrounds the wafer during the rie etching process, and is used to scavenge free F in the plasma etchant; and

-the specific usage of applicant's claimed etching process parameters

It would have been obvious to one skilled in the art to replace the Si3N4 etch stop layer in the process taught above with a TiN etch stop layer based upon the following. The usage of TiN etch stop layers when etching vias in SiO2 ILD layers is conventional or at least well known in the semiconducting arts. (The examiner takes official notice in this regard.) Further, this simply provides an alternative, and at least equivalent means for providing a nitride etch stop means in etching process taught above to those means which are specifically taught above (i.e.- a Si3N4 etch stop.)

It would have been obvious to one skilled in the art to equip the rie etching apparatus employed in the plasma etching process taught above with a solid Si electrode which forms the roof of the plasma etching chamber based upon the following. The usage of such a solid Si electrode to scavenge free fluorine in a fluorocarbon based plasma used to selectively rie etch an oxide layer to a nitride layer is conventional or at least well known in the plasma etching arts. (The examiner takes official notice in this regard.) Further, this would simply provide a means

for further desirably increasing the etch selectivity of the oxide based layer to the nitride based layer in the etching process taught above by scavenging free fluorine in the plasma etchant.

It would have been obvious to one skilled in the art to employ a Si ring on the cathode in the rie etcher taught above during the rie etching process based upon the following. The usage of a Si ring on a cathode which surrounds a wafer to be etched in a fluorocarbon based plasma during the selective etching of an oxide based layer to a nitride based layer is conventional or at least well known in the etching arts. (The examiner takes official notice in this regard.) Further, this would simply provide a means for further desirably increasing the etch selectivity of the oxide based layer to the nitride based layer in the etching process taught above.

It would have been prima facie obvious to employ any of a variety of different etch process parameters in the etching process taught above including those which are specifically claimed by the applicant. These are all well known variables in the plasma etching art which are known to effect both the rate and quality of the plasma etching process. Further, the selection of particular values for these variables would not necessitate any undo experimentation which would be indicative of a showing of unexpected results.

Alternatively, it would have been obvious to one skilled in the art to employ the specific etch process parameters which are claimed by the applicant in the etching process taught above based upon In re Aller as cited below.

"Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F. 2d 454, 105 USPQ 233, 235 (CCPA).

Further, all of the specific etching process parameters which are claimed by the applicant are results effective variables whose values are known to effect both the rate, and the quality of the plasma etching process.

30. Claims 3-5, 8, 10-13, 21, and 23-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nulty as applied in paragraph 21 above.

Nulty as applied in paragraph 21 above fail to disclose the following aspects of applicant's claimed invention:

-the specific usage of TiN as the etch stop layer in place of the Si3N4 etch stop layer specifically taught above;

-the specific usage of a solid Si electrode (i.e.-a Si roof in the plasma etching chamber) to scavenge free F in the plasma etchant during the plasma etching process;

-the specific usage of a Si ring on the cathode in the rie etcher which surrounds the wafer during the rie etching process, and is used to scavenge free F in the plasma etchant; and

-the specific usage of applicant's claimed etching process parameters

It would have been obvious to one skilled in the art to replace the Si3N4 etch stop layer in the process taught above with a TiN etch stop layer based upon the following. The usage of TiN

etch stop layers when etching vias in SiO2 ILD layers is conventional or at least well known in the semiconducting arts. (The examiner takes official notice in this regard.) Further, this simply provides an alternative, and at least equivalent means for providing a nitride etch stop means in etching process taught above to those means which are specifically taught above (i.e.- a Si3N4 etch stop.)

It would have been obvious to one skilled in the art to equip the rie etching apparatus employed in the plasma etching process taught above with a solid Si electrode which forms the roof of the plasma etching chamber based upon the following. The usage of such a solid Si electrode to scavenge free fluorine in a fluorocarbon based plasma used to selectively rie etch an oxide layer to a nitride layer is conventional or at least well known in the plasma etching arts. (The examiner takes official notice in this regard.) Further, this would simply provide a means for further desirably increasing the etch selectivity of the oxide based layer to the nitride based layer in the etching process taught above by scavenging free fluorine in the plasma etchant.

It would have been obvious to one skilled in the art to employ a Si ring on the cathode in the rie etcher taught above during the rie etching process based upon the following. The usage of a Si ring on a cathode which surrounds a wafer to be etched in a fluorocarbon based plasma during the selective etching of an oxide based layer to a nitride based layer is conventional or at least well known in the etching arts. (The examiner takes official notice in this regard.) Further,

this would simply provide a means for further desirably increasing the etch selectivity of the oxide based layer to the nitride based layer in the etching process taught above.

It would have been prima facie obvious to employ any of a variety of different etch process parameters in the etching process taught above including those which are specifically claimed by the applicant. These are all well known variables in the plasma etching art which are known to effect both the rate and quality of the plasma etching process. Further, the selection of particular values for these variables would not necessitate any undo experimentation which would be indicative of a showing of unexpected results.

Alternatively, it would have been obvious to one skilled in the art to employ the specific etch process parameters which are claimed by the applicant in the etching process taught above based upon In re Aller as cited below.

"Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F. 2d 454, 105 USPQ 233, 235 (CCPA).

Further, all of the specific etching process parameters which are claimed by the applicant are results effective variables whose values are known to effect both the rate, and the quality of the plasma etching process.

31. Claims 4, 8, 21, 23-25, 29, 32-33, 35, and 42-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Marquez et. al. as applied in paragraph 22 above.

Marquez et. al. as applied in paragraph 22 above fail to disclose the following aspects of applicant's claimed invention:

-the specific usage of TiN as the etch stop layer in place of the Si3N4 etch stop layer specifically taught above;

-the specific usage of a solid Si electrode (i.e.-a Si roof in the plasma etching chamber) to scavenge free F in the plasma etchant during the plasma etching process;

-the specific usage of a Si ring on the cathode in the rie etcher which surrounds the wafer during the rie etching process, and is used to scavenge free F in the plasma etchant; and

-the specific usage of applicant's claimed etching process parameters

It would have been obvious to one skilled in the art to replace the Si3N4 etch stop layer in the process taught above with a TiN etch stop layer based upon the following. The usage of TiN etch stop layers when etching vias in SiO2 ILD layers is conventional or at least well known in the semiconducting arts. (The examiner takes official notice in this regard.) Further, this simply provides an alternative, and at least equivalent means for providing a nitride etch stop means in etching process taught above to those means which are specifically taught above (i.e.- a Si3N4 etch stop.)

It would have been obvious to one skilled in the art to equip the rie etching apparatus employed in the plasma etching process taught above with a solid Si electrode which forms the roof of the plasma etching chamber based upon the following. The usage of such a solid Si electrode to scavenge free fluorine in a fluorocarbon based plasma used to selectively rie etch an oxide layer to a nitride layer is conventional or at least well known in the plasma etching arts. (The examiner takes official notice in this regard.) Further, this would simply provide a means for further desirably increasing the etch selectivity of the oxide based layer to the nitride based layer in the etching process taught above by scavenging free fluorine in the plasma etchant.

It would have been obvious to one skilled in the art to employ a Si ring on the cathode in the rie etcher taught above during the rie etching process based upon the following. The usage of a Si ring on a cathode which surrounds a wafer to be etched in a fluorocarbon based plasma during the selective etching of an oxide based layer to a nitride based layer is conventional or at least well known in the etching arts. (The examiner takes official notice in this regard.) Further, this would simply provide a means for further desirably increasing the etch selectivity of the oxide based layer to the nitride based layer in the etching process taught above.

It would have been prima facie obvious to employ any of a variety of different etch process parameters in the etching process taught above including those which are specifically claimed by the applicant. These are all well known variables in the plasma etching art which are known to effect both the rate and quality of the plasma etching process. Further, the selection of

particular values for these variables would not necessitate any undo experimentation which would be indicative of a showing of unexpected results.

Alternatively, it would have been obvious to one skilled in the art to employ the specific etch process parameters which are claimed by the applicant in the etching process taught above based upon In re Aller as cited below.

"Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F. 2d 454, 105 USPQ 233, 235 (CCPA).

Further, all of the specific etching process parameters which are claimed by the applicant are results effective variables whose values are known to effect both the rate, and the quality of the plasma etching process.

32. Claims 4-5, 8, 11-12, and 36-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuo et. al. as applied in paragraph 23 above.

Kuo et. al. as applied in paragraph 23 above fail to disclose the following aspects of applicant's claimed invention:

-the specific usage of a solid Si electrode (i.e.-a Si roof in the plasma etching chamber) to scavenge free F in the plasma etchant during the plasma etching process;

-the specific usage of a Si ring on the cathode in the rie etcher which surrounds the wafer during the rie etching process, and is used to scavenge free F in the plasma etchant; and

-the specific usage of applicant's claimed etching process parameters

It would have been obvious to one skilled in the art to equip the rie etching apparatus employed in the plasma etching process taught above with a solid Si electrode which forms the roof of the plasma etching chamber based upon the following. The usage of such a solid Si electrode to scavenge free fluorine in a fluorocarbon based plasma used to selectively rie etch an oxide layer to a nitride layer is conventional or at least well known in the plasma etching arts. (The examiner takes official notice in this regard.) Further, this would simply provide a means for further desirably increasing the etch selectivity of the oxide based layer to the nitride based layer in the etching process taught above by scavenging free fluorine in the plasma etchant.

It would have been obvious to one skilled in the art to employ a Si ring on the cathode in the rie etcher taught above during the rie etching process based upon the following. The usage of a Si ring on a cathode which surrounds a wafer to be etched in a fluorocarbon based plasma during the selective etching of an oxide based layer to a nitride based layer is conventional or at least well known in the etching arts. (The examiner takes official notice in this regard.) Further, this would simply provide a means for further desirably increasing the etch selectivity of the oxide based layer to the nitride based layer in the etching process taught above.

It would have been prima facie obvious to employ any of a variety of different etch process parameters in the etching process taught above including those which are specifically claimed by the applicant. These are all well known variables in the plasma etching art which are

known to effect both the rate and quality of the plasma etching process. Further, the selection of particular values for these variables would not necessitate any undo experimentation which would be indicative of a showing of unexpected results.

Alternatively, it would have been obvious to one skilled in the art to employ the specific etch process parameters which are claimed by the applicant in the etching process taught above based upon In re Aller as cited below.

"Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F. 2d 454, 105 USPQ 233, 235 (CCPA).

Further, all of the specific etching process parameters which are claimed by the applicant are results effective variables whose values are known to effect both the rate, and the quality of the plasma etching process.

33. Claims 4, 8, 10-12, 36, and 39-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et. al. as applied in paragraph 20 above.

Lin et. al. as applied in paragraph 20 above fail to disclose the following aspects of applicant's claimed invention:

It would have been obvious to one skilled in the art to equip the rie etching apparatus employed in the plasma etching process taught above with a solid Si electrode which forms the roof of the plasma etching chamber based upon the following. The usage of such a solid Si

electrode to scavenge free fluorine in a fluorocarbon based plasma used to selectively rie etch an oxide layer to a nitride layer is conventional or at least well known in the plasma etching arts. (The examiner takes official notice in this regard.) Further, this would simply provide a means for further desirably increasing the etch selectivity of the oxide based layer to the nitride based layer in the etching process taught above by scavenging free fluorine in the plasma etchant.

It would have been obvious to one skilled in the art to employ a Si ring on the cathode in the rie etcher taught above during the rie etching process based upon the following. The usage of a Si ring on a cathode which surrounds a wafer to be etched in a fluorocarbon based plasma during the selective etching of an oxide based layer to a nitride based layer is conventional or at least well known in the etching arts. (The examiner takes official notice in this regard.) Further, this would simply provide a means for further desirably increasing the etch selectivity of the oxide based layer to the nitride based layer in the etching process taught above.

It would have been prima facie obvious to employ any of a variety of different etch process parameters in the etching process taught above including those which are specifically claimed by the applicant. These are all well known variables in the plasma etching art which are known to effect both the rate and quality of the plasma etching process. Further, the selection of particular values for these variables would not necessitate any undo experimentation which would be indicative of a showing of unexpected results.

Alternatively, it would have been obvious to one skilled in the art to employ the specific etch process parameters which are claimed by the applicant in the etching process taught above based upon In re Aller as cited below.

"Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F. 2d 454, 105 USPQ 233, 235 (CCPA).

Further, all of the specific etching process parameters which are claimed by the applicant are results effective variables whose values are known to effect both the rate, and the quality of the plasma etching process.

34. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner George A. Goudreau whose telephone number is (703) -308-1915. The examiner can normally be reached on Monday through Friday from 9:30 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Examiner Gregory Mills, can be reached on (703) -308-1633. The appropriate fax phone number for the organization where this application or proceeding is assigned is (703) -306-3186.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) -308-0661.

George A. Goudreau/gag

Primary Examiner

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